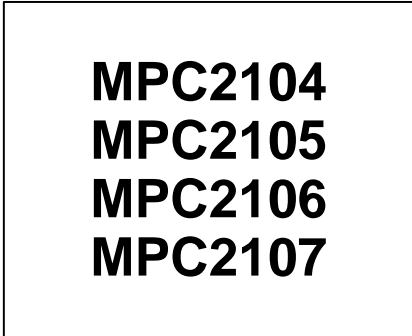


Advance Information

256KB and 512KB BurstRAM™ Secondary Cache Modules for PowerPC™ PReP/CHRP Platforms



The MPC2104/5/6/7 are designed to provide burstable, high performance L2 cache for the PowerPC 60x microprocessor family in conformance with the PowerPC Reference Platform (PReP) and the PowerPC Common Hardware Reference Platform (CHRP) specifications. These products utilize synchronous or asynchronous data RAMs.

The MPC2104, MPC2105, and MPC2106 utilize synchronous BurstRAMs. The modules are configured as 32K x 72, 64K x 72, and 128K x 72 bits in a 182 (91 x 2) pin DIMM format. The MPC2104 uses four of Motorola's 5 V 32K x 18; the MPC2105 uses four of the 5 V 64K x 18; the MPC2106 uses eight of the 5 V 64K x 18. For tag bits, a 5 V cache tag RAM configured as 16K x 12 for tag field plus 16K x 2 for valid and dirty status bits is used.

Bursts can be initiated with the ADS signal. Subsequent burst addresses are generated internal to the BurstRAM by the CNTEN signal.

Write cycles are internally self timed and are initiated by the rising edge of the clock (CLKx) inputs. Eight write enables are provided for byte write control.

The MPC2107 utilizes asynchronous data RAMs. The module is configured as 32K x 64 in the same 182 pin DIMM format. Again, 5 V cache tag RAMs configured as 16K x 12 for tag field plus 16K x 2 for valid and dirty status bits are used. Burst capability is provided in that two burst addresses bypass the address latch.

Presence detect pins are available for auto configuration of the cache control. A serial EEPROM is optional to provide more in-depth description of the cache module. This EEPROM will be available on future revisions of the module family.

The module family pinout will support 5 V and 3.3 V components for a clear path to lower voltage and power savings. Both power supplies must be connected.

All of these cache modules are plug and pin compatible with each other.

- PowerPC-style Burst Counter on Chip (MPC2104/5/6)
- Flow-Through Data I/O (MPC2104/5/6)
- Plug and Pin Compatibility of entire Module Family
- Multiple Clock Pins for Reduced Loading
- All Cache Data and Tag I/Os are LVTTTL (3.3 V) Compatible (MPC2104/5/6)
- Three State Outputs
- Byte Write Capability
- Fast Module Clock Rates: Up to 66 MHz
- Fast SRAM Access Times: 10 ns for Tag RAM Match
9 ns for Data RAM (MPC2104/5/6)
15 ns for Data RAM (MPC2107)
- Decoupling Capacitors for Each Fast Static RAM
- High Quality Multi-Layer FR4 PWB With Separate Power and Ground Planes
- 182 Pin Card Edge Module
- Burndy Connector, Part Number: ELF182JSC-3Z50

BurstRAM is a trademark of Motorola.

PowerPC is a trademark of International Business Machines Corp.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

11/8/95

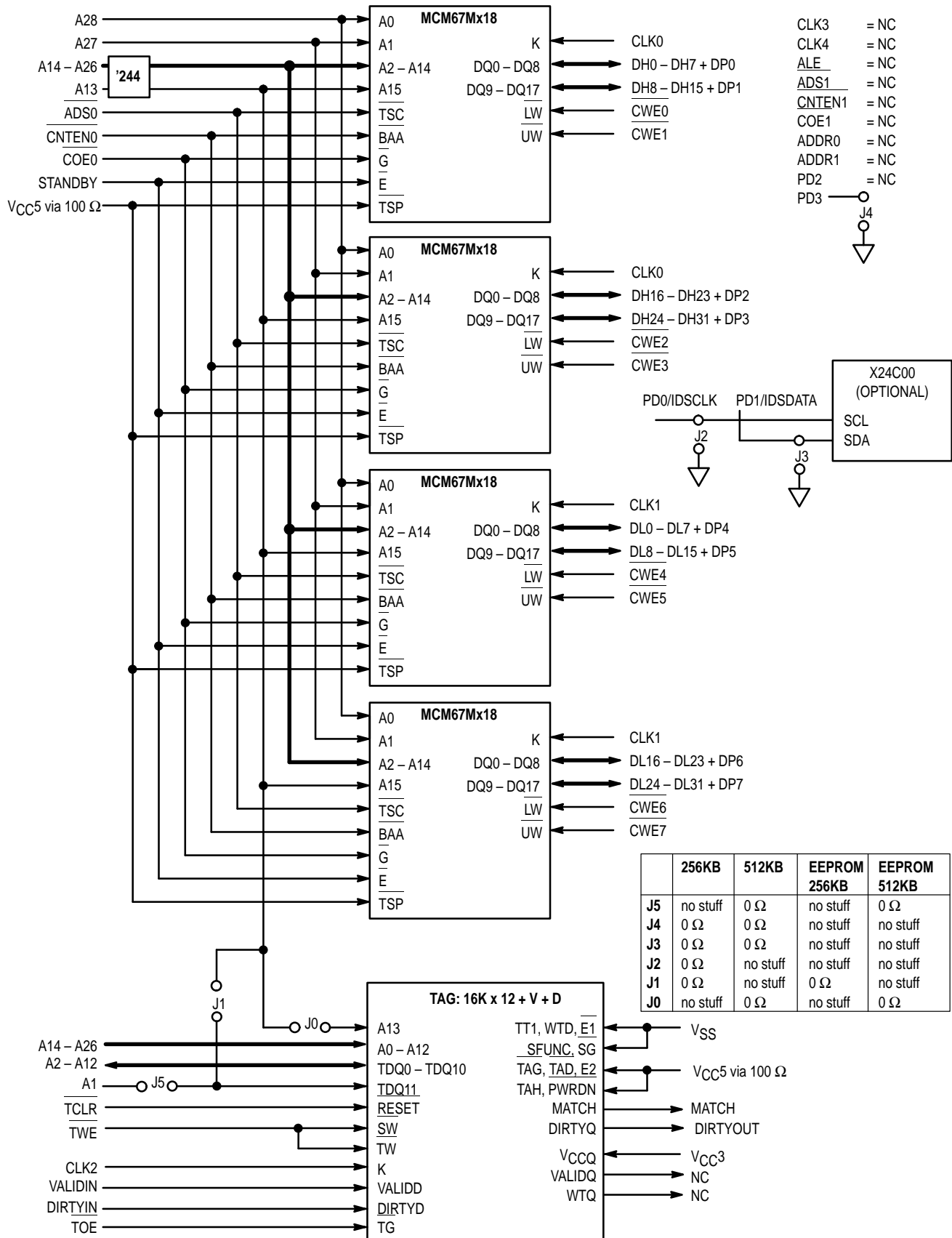
**PIN ASSIGNMENT
182-LEAD DIMM
TOP VIEW – CASE TBD**

| | | | |
|-------------|-----|----|-----------|
| VSS | 92 | 1 | VSS |
| PD1/IDSDATA | 93 | 2 | PD0/IDCLK |
| PD3 | 94 | 3 | PD2 |
| DH31 | 95 | 4 | DH30 |
| DH29 | 96 | 5 | DH28 |
| DH27 | 97 | 6 | DH26 |
| DH25 | 98 | 7 | DH24 |
| VCC3 | 99 | 8 | VCC3 |
| CWE3 | 100 | 9 | DP3 |
| DH23 | 101 | 10 | DH22 |
| DH21 | 102 | 11 | DH20 |
| DH18 | 103 | 12 | DH19 |
| VSS | 104 | 13 | VSS |
| DH16 | 105 | 14 | DH17 |
| CWE2 | 106 | 15 | DP2 |
| DH14 | 107 | 16 | DH15 |
| DH13 | 108 | 17 | DH12 |
| VCC5 | 109 | 18 | VCC5 |
| DH10 | 110 | 19 | DH11 |
| DH8 | 111 | 20 | DH9 |
| CWE1 | 112 | 21 | DP1 |
| DH6 | 113 | 22 | DH7 |
| VCC3 | 114 | 23 | VCC3 |
| DH4 | 115 | 24 | DH5 |
| VSS | 116 | 25 | DH3 |
| CLK0 | 117 | 26 | DH2 |
| VSS | 118 | 27 | DH0 |
| DH1 | 119 | 28 | DP0 |
| CWE0 | 120 | 29 | VSS |
| DL31 | 121 | 30 | CLK1 |
| DL30 | 122 | 31 | VSS |
| VSS | 123 | 32 | DL28 |
| DL29 | 124 | 33 | DL26 |
| DL27 | 125 | 34 | DL24 |
| DL25 | 126 | 35 | DP7 |
| VCC5 | 127 | 36 | VCC5 |
| CWE7 | 128 | 37 | DL22 |
| DL23 | 129 | 38 | DL20 |
| DL21 | 130 | 39 | DL18 |
| DL19 | 131 | 40 | DL16 |
| VSS | 132 | 41 | VSS |
| DL17 | 133 | 42 | DP6 |
| CWE6 | 134 | 43 | DL14 |
| DL15 | 135 | 44 | DL12 |
| DL13 | 136 | 45 | DL11 |
| VSS | 137 | 46 | VSS |
| DL10 | 138 | 47 | DL9 |
| DL8 | 139 | 48 | DP5 |
| CWE5 | 140 | 49 | DL7 |
| DL6 | 141 | 50 | DL4 |
| VCC3 | 142 | 51 | VCC3 |
| DL5 | 143 | 52 | DL3 |
| DL2 | 144 | 53 | DL1 |
| VSS | 145 | 54 | DL0 |
| CLK3 | 146 | 55 | VSS |
| VSS | 147 | 56 | CLK2 |
| CLK4 | 148 | 57 | VSS |
| VSS | 149 | 58 | DP4 |
| CWE4 | 150 | 59 | COE0 |
| ALE | 151 | 60 | COE1 |
| VCC3 | 152 | 61 | VCC3 |
| ADDR1 | 153 | 62 | ADDR0 |
| RESERVED | 154 | 63 | RESERVED |
| CNTEN0 | 155 | 64 | ADS0 |
| CNTEN1 | 156 | 65 | ADS1 |
| VCC5 | 157 | 66 | VCC5 |
| VCC5 | 158 | 67 | VCC5 |
| A27 | 159 | 68 | A28 |
| A24 | 160 | 69 | A26 |
| A22 | 161 | 70 | A25 |
| A20 | 162 | 71 | A23 |
| VSS | 163 | 72 | VSS |
| A18 | 164 | 73 | A21 |
| A16 | 165 | 74 | A19 |
| A15 | 166 | 75 | A17 |
| A14 | 167 | 76 | A13 |
| VCC3 | 168 | 77 | VCC3 |
| A10 | 169 | 78 | A12 |
| A8 | 170 | 79 | A11 |
| A6 | 171 | 80 | A9 |
| VSS | 172 | 81 | VSS |
| A4 | 173 | 82 | A7 |
| A2 | 174 | 83 | A5 |
| A1 | 175 | 84 | A3 |
| BURSTMODE | 176 | 85 | A0 |
| VCC5 | 177 | 86 | VCC5 |
| VALIDIN | 178 | 87 | TCLR |
| TWE | 179 | 88 | MATCH |
| STANDBY | 180 | 89 | TOE |
| DIRTYOUT | 181 | 90 | DIRTYIN |
| VSS | 182 | 91 | VSS |

NOTES:

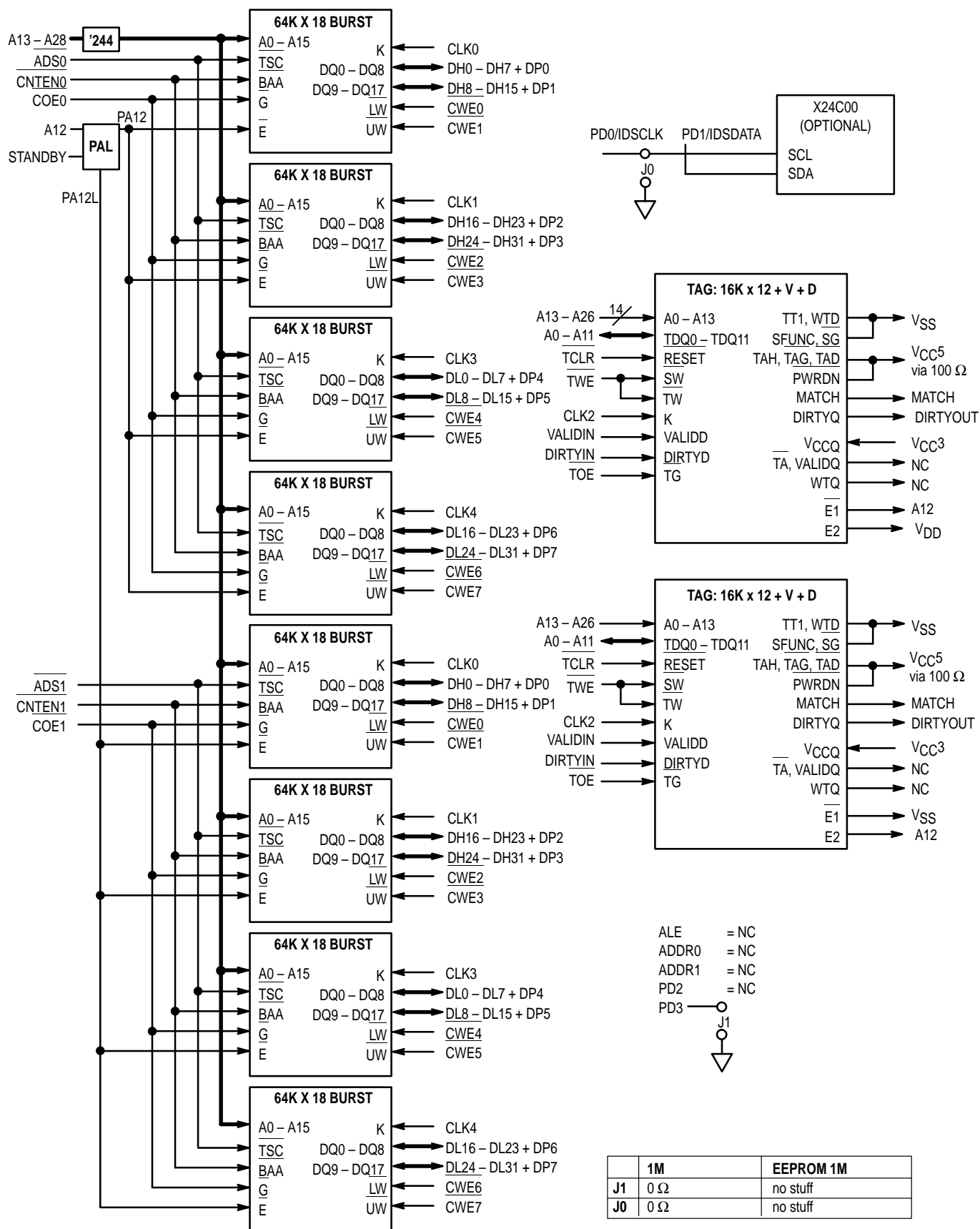
1. VCC5 and VCC3 must be connected on all modules.

MPC2104/MPC2105 BLOCK DIAGRAM



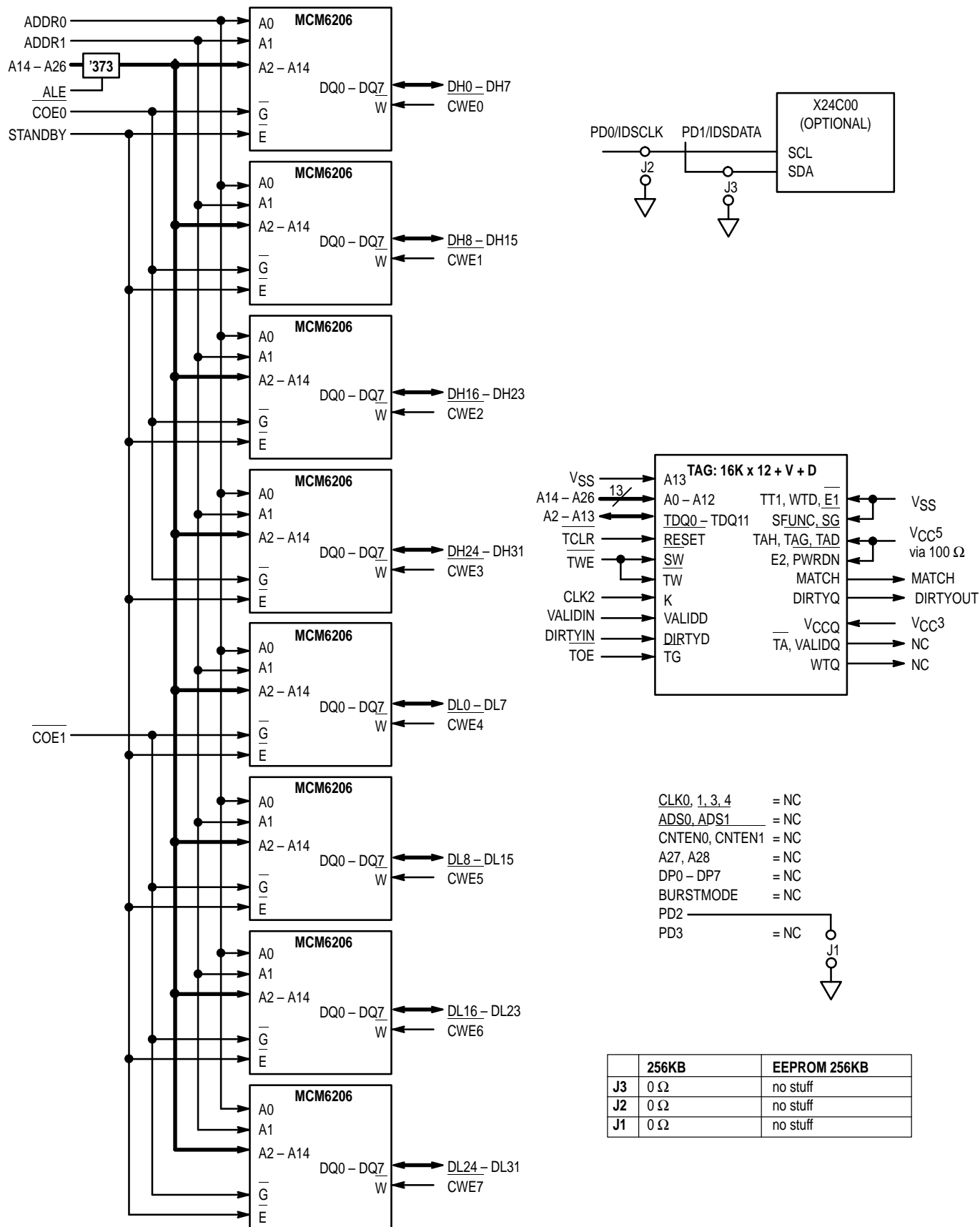
Note: MPC2104 utilizes 32K x 18 BurstRAMs. MPC2105 utilizes 64K x 18 BurstRAMs.

MPC2106 BLOCK DIAGRAM



Note: All 64K X 18 TSP signals are tied to V_{CC} via a 100 Ω resistor. Edge connector A28 connects to the 64K x 18 A0; edge connector A27 connects to the 64K x 18 A1.

MPC2107 BLOCK DIAGRAM



| | 256KB | EEPROM 256KB |
|----|-------|--------------|
| J3 | 0 Ω | no stuff |
| J2 | 0 Ω | no stuff |
| J1 | 0 Ω | no stuff |

PIN DESCRIPTIONS

| Pin Locations | Symbol | Type | Description |
|--|----------------|--------|---|
| 68, 69, 70, 71, 73, 74, 75, 76, 78, 79, 80, 82, 83, 84, 85, 159, 160, 161, 162, 164, 165, 166, 167, 169, 170, 171, 173, 174, 175 | A0 – A28 | Input | Address Inputs – (MSB:0, LSB:28) |
| 62 | ADDR0 | Input | Least significant address bit when asynchronous Data RAMs are used. |
| 153 | ADDR1 | Input | Next to least significant address bit when asynchronous Data RAMs are used. |
| 30, 56, 117, 146, 148 | CLK0 – CLK4 | Input | Clock Inputs – CLK2 is for Tag RAM, CLK0, 1, 3, and 4 are for Data RAMs only. For MPC2106 use all the clocks. For MPC2104 or MPC2105 use CLK0–CLK2 only. For MPC2107 use CLK2 only. |
| 4, 5, 6, 7, 10, 11, 12, 14, 16, 17, 19, 20, 22, 24, 25, 26, 27, 95, 96, 97, 98, 101, 102, 103, 105, 107, 108, 110, 111, 113, 115, 119 | DH0 – DH31 | I/O | High Data Bus – (MSB:0, LSB:31) |
| 32, 33, 34, 37, 38, 39, 40, 43, 44, 45, 47, 49, 50, 52, 53, 54, 121, 122, 124, 125, 126, 129, 130, 131, 133, 135, 136, 138, 139, 141, 143, 144 | DL0 – DL31 | I/O | Low Data Bus – (MSB:0, LSB:31) |
| 9, 15, 21, 28, 35, 42, 48, 58 | DP0 – DP7 | I/O | Data Parity Bits – (MSB:0, LSB:7) |
| 3, 94 | PD2, PD3 | Output | Presence detect bits. |
| 2 | PD0/IDSCLK | Input | Presence detect bit 0/EEPROM serial clock. (EEPROM option only.) |
| 93 | PD1/IDSDATA | I/O | Presence detect bit 1/EEPROM serial data. (EEPROM option only.) |
| 64, 65 | ADS0, ADS1 | Input | Data RAM Address Strobe – For MPC2104 or MPC2105 use ADS0 only. For MPC2106 use ADS0, ADS1. |
| 151 | ALE | Input | Data RAM Address Latch Enable – Use for asynchronous Data RAM only. |
| 155, 156 | CNTEN0, CNTEN1 | Input | Data RAM Count Enables – For MPC2104 or MPC2105 use CNTEN0 only. For MPC2106 use CNTEN0, CNTEN1. |
| 59, 60 | COE0, COE1 | Input | Data RAM Output Enables – For MPC2104 or MPC2105 use COE0 only. For all others use COE0, COE1. |
| 100, 106, 112, 120, 128, 134, 140, 150 | CWE0 – CWE7 | Input | Data RAM Write Enables – (MSB:0, LSB:7) |
| 87 | TCLR | Input | Tag RAM clear. |
| 88 | MATCH | Output | Tag RAM active high match indication. |
| 178 | VALIDIN | Input | Tag RAM valid bit. |
| 179 | TWE | Input | Tag RAM write enable. |
| 89 | TOE | Input | Tag RAM output enable. |
| 90 | DIRTYIN | Input | Dirty input bit. |
| 181 | DIRTYOUT | Output | Dirty output bit. |
| 180 | STANDBY | Input | Standby pin. Reduces standby power consumption. |
| 176, 63, 154 | RESERVED | | Reserved pin. |
| 8, 23, 51, 61, 77, 99, 114, 142, 152, 168 | VCC3 | Input | + 3.3 V power supply. Must be connected. |
| 18, 36, 66, 67, 86, 109, 127, 157, 158, 177 | VCC5 | Input | + 5 V power supply. Must be connected. |
| 1, 13, 29, 31, 41, 46, 55, 57, 72, 81, 91, 92, 104, 116, 118, 123, 132, 137, 145, 147, 149, 163, 172, 182 | VSS | Input | Ground |
| 176 | BURSTMODE | Input | Burstmode. 0 = Linear, 1 = Interleaved. |

DATA RAM MCM67M518, MCM67M618 SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

| STANDBY | ADS0 | CNTEN0 | CWEx | CLKx | Address Used | Operation |
|---------|------|--------|------|------|------------------|-----------------------------|
| H | L | X | X | L-H | N/A | Deselected |
| L | L | X | L | L-H | External Address | Write Cycle, Begin Burst |
| L | L | X | H | L-H | External Address | Read Cycle, Begin Burst |
| X | H | L | L | L-H | Next Address | Write Cycle, Continue Burst |
| X | H | L | H | L-H | Next Address | Read Cycle, Continue Burst |
| X | H | H | L | L-H | Current Address | Write Cycle, Suspend Burst |
| X | H | H | H | L-H | Current Address | Read Cycle, Suspend Burst |

NOTES:

1. X means Don't Care.
2. All inputs except COE must meet set-up and hold times for the low-to-high transition of clock (CLK0 – CLK4).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

| Operation | COE | I/O Status |
|------------|-----|----------------------|
| Read | L | Data Out (DQ0 – DQ8) |
| Read | H | High-Z |
| Write | X | High-Z — Data In |
| Deselected | X | High-Z |

NOTES:

1. X means Don't Care.
2. For a write operation following a read operation, COE must be high before the input data required set-up time and held high through the input data hold time.

DATA RAM MCM6206 ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

| STANDBY | COE0, COE1 | CWE0 – CWE7 | Operation | I/O Status |
|---------|------------|-------------|-----------------|------------|
| H | X | X | Deselected | High-Z |
| L | H | H | Output Disabled | High-Z |
| L | L | H | Read | Data Out |
| L | X | L | Write | High-Z |

NOTES:

1. X means Don't Care.
2. For a write operation following a read operation, COE0, and COE1 must be high before the input data required set-up time, and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to $V_{SS} = 0$ V)

| Rating | Symbol | Value | Unit |
|------------------------------|---------------------------|-------------------------|------|
| Power Supply Voltage | V_{CC} | - 0.5 to + 7.0 | V |
| Voltage Relative to V_{SS} | V_{in}, V_{out} | - 0.5 to $V_{CC} + 0.5$ | V |
| Output Current (per I/O) | Data RAM Tag I_{out} | ± 30 ± 20 | mA |
| Power Dissipation | P_D | 8.1 | W |
| Temperature Under Bias | T_{bias} | - 10 to + 85 | °C |
| Operating Temperature | T_A | 0 to +70 | °C |
| Storage Temperature | T_{stg} | - 55 to + 125 | °C |

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High-Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = 5.0\text{ V} \pm 5\%$, $T_A = 0\text{ to } +70^\circ\text{C}$, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS} = 0\text{ V}$)

| Parameter | Symbol | Min | Max | Unit |
|--|----------|----------|---------------------|------|
| Supply Voltage (Operating Voltage Range) | V_{CC} | 4.75 | 5.25 | V |
| Input High Voltage | V_{IH} | 2.2 | $V_{CC} + 0.3^{**}$ | V |
| Input Low Voltage | V_{IL} | -0.5^* | 0.8 | V |

* $V_{IL}(\text{min}) = -0.5\text{ V dc}$; $V_{IL}(\text{min}) = -2.0\text{ V ac}$ (pulse width $\leq 20\text{ ns}$) for $I \leq 20.0\text{ mA}$.

** $V_{IH}(\text{max}) = V_{CC} + 0.3\text{ V dc}$; $V_{IH}(\text{max}) = V_{CC} + 2.0\text{ V ac}$ (pulse width $\leq 20\text{ ns}$) for $I \leq 20.0\text{ mA}$.

DC CHARACTERISTICS

| Parameter | Symbol | Min | Max | Unit |
|--|---------------------------------|-----|------------------------|---------------|
| Input Leakage Current (All Inputs, $V_{in} = 0\text{ to } V_{CC}$) | Data RAM Tag $I_{lkg(I)}$ | — | ± 1.0 ± 5.0 | μA |
| Output Leakage Current (COE = V_{IH} , $V_{out} = 0\text{ to } V_{CC}$) | Data RAM Tag $I_{lkg(O)}$ | — | ± 1.0 ± 5.0 | μA |
| TTL Output Low Voltage ($I_{OL} = +8.0\text{ mA}$) | V_{OL} | — | 0.4 | V |
| TTL Output High Voltage ($I_{OH} = -4.0\text{ mA}$) | V_{OH} | 2.4 | — | V |

POWER SUPPLY CURRENTS

| Parameter | Symbol | Max | Unit |
|--|---|------------------------------|------|
| AC Supply Current (COE = V_{IH} , $E = V_{IL}$, $I_{out} = 0\text{ mA}$, All Inputs = V_{IL} and V_{IH} , $V_{IL} = 0.0\text{ V}$ and $V_{IH} \geq 3.0\text{ V}$, Cycle Time $\geq 20\text{ ns}$) | MPC2104 MPC2105 MPC2106 MPC2107 I_{CCA} | 1480 1420 2840 1400 | mA |
| AC Standby Current ($E = V_{IH}$, $I_{out} = 0\text{ mA}$, All Inputs = V_{IL} or V_{IH} , $V_{IL} = 0.0\text{ V}$ and $V_{IH} \geq 3.0\text{ V}$, Cycle Time $\geq 20\text{ ns}$) | MPC2104 MPC2105 MPC2106 MPC2107 I_{SB1} | 620 700 1400 960 | mA |

CAPACITANCE ($f = 1.0\text{ MHz}$, $dV = 3.0\text{ V}$, $T_A = 25^\circ\text{C}$, Periodically Sampled Rather Than 100% Tested)

| Parameter | Symbol | Typ | Max | Unit |
|--|-----------|-------------------|---------------------|------|
| Input Capacitance (A13 – A28) (Data RAM Control Pins) (CLK0 – CLK4) (Tag Control Pins) | C_{in} | — 16 8 — | 15 20 10 5 | pF |
| Tag Output Capacitance (MATCH, DIRTYOUT) | C_{out} | — | 7 | pF |
| Data RAM Input/Output Capacitance (DH0 – DH31, DL0 – DL31) | $C_{I/O}$ | 6 | 8 | pF |
| Tag Input/Output Capacitance (A0 – A11) | $C_{I/O}$ | — | 7 | pF |

DATA RAMs AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5% T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level 1.5 V
 Input Pulse Levels 0 to 3.0 V
 Input Rise/Fall Time 3 ns

Output Timing Reference Level 1.5 V
 Output Load See Figure 1A Unless Otherwise Noted

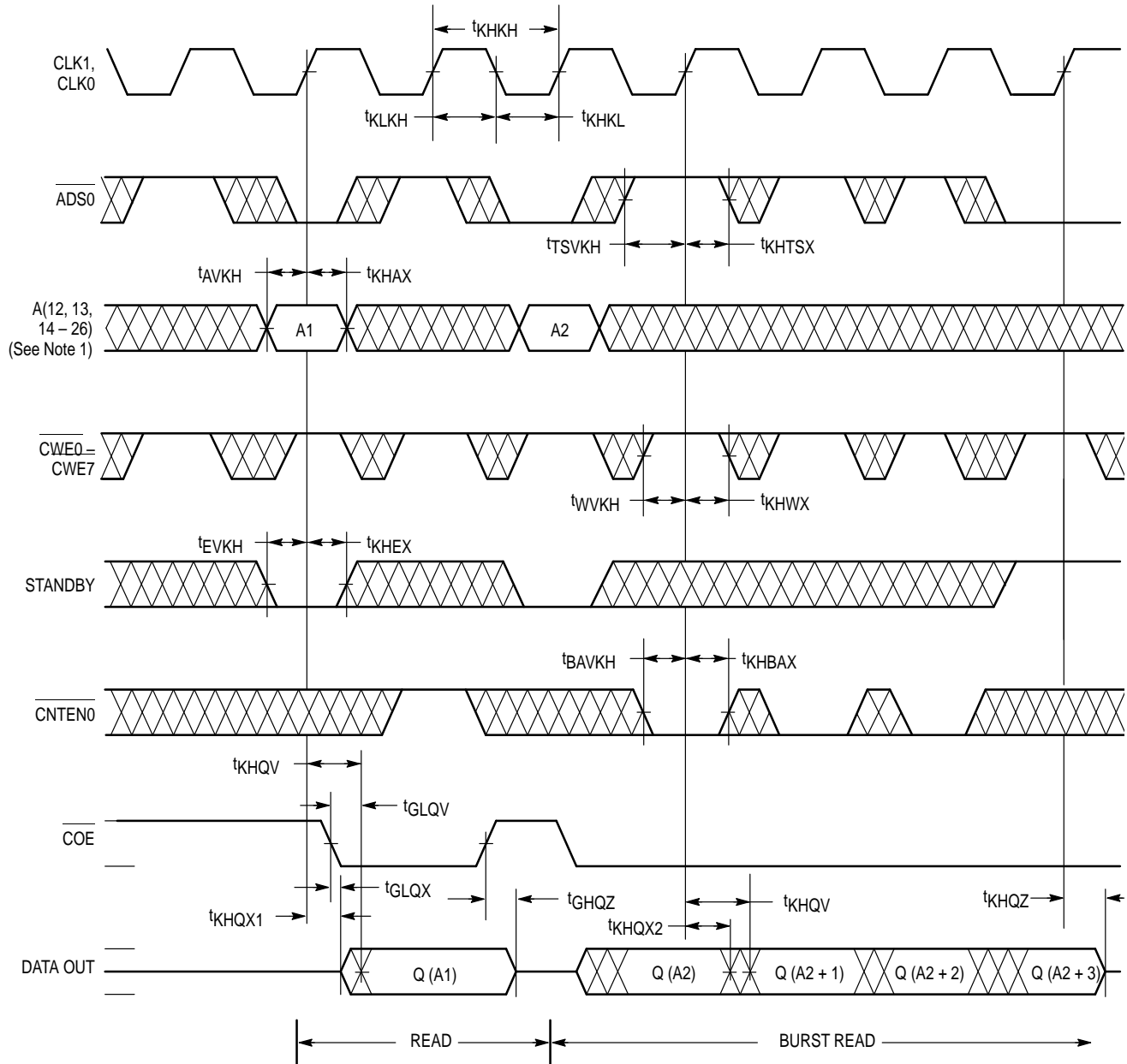
SYNCHRONOUS DATA RAMs READ/WRITE CYCLE TIMING (See Notes 1, 2, 3, and 7)

| Parameter | Symbol | MPC2104 MPC2105 MPC2106 | | Unit | Notes |
|--------------------------------|-------------------------------------|-------------------------------|-----|------|-------|
| | | Min | Max | | |
| Cycle Time | t _{KHKH} | 15 | — | ns | |
| Clock Access Time | t _{KHQV} | — | 9 | ns | 4 |
| Output Enable to Output Valid | t _{GLQV} | — | 5 | ns | |
| Clock High to Output Active | t _{KHQX1} | 6 | — | ns | |
| Clock High to Output Change | t _{KHQX2} | 3 | — | ns | |
| Output Enable to Output Active | t _{GLQX} | 0 | — | ns | |
| Output Disable to Q High-Z | t _{GHQZ} | 2 | 6 | ns | |
| Clock High to Q High-Z | t _{KHQZ} | — | 6 | ns | |
| Clock High Pulse Width | t _{KHKL} | 5 | — | ns | |
| Clock Low Pulse Width | t _{KLKH} | 5 | — | ns | |
| Setup Time | Address t _{AVKH} | 7.5 | — | ns | 5, 6 |
| Setup Times: | Address Status t _{SVKH} | 2.5 | — | ns | 5 |
| | Data In t _{DVKH} | | | | |
| | Write t _{WVKH} | | | | |
| | Address Advance t _{BAVVKH} | | | | |
| | Chip Enable t _{EVKH} | | | | |
| Hold Times: | Address t _{KHAX} | 0.5 | — | ns | 5 |
| | Address Status t _{KHTSX} | | | | |
| | Data In t _{KHDX} | | | | |
| | Write t _{KHWX} | | | | |
| | Address Advance t _{KHBAX} | | | | |
| | Chip Enable t _{KHEX} | | | | |

NOTES:

1. In setup and hold times, W (write) refers to either one or both byte write enables LW and UW.
2. All read and write cycle timings are referenced from CLK or COE.
3. COE is a don't care when UW or LW is sampled low.
4. Maximum access times are guaranteed for all possible PowerPC external bus cycles.
5. This is a synchronous device. All addresses must meet the specified setup and hold times for **ALL** rising edges of CLK whenever TSP or TSC is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for **ALL** rising edges of CLK when the chip is enabled. Chip enable must be valid at each rising edge of clock for the device (when TSP or TSC is low) to remain enabled.
6. 5 ns of set-up delay is incurred in address buffers.
7. Applies to MPC2104, MPC2105, and MPC2106.

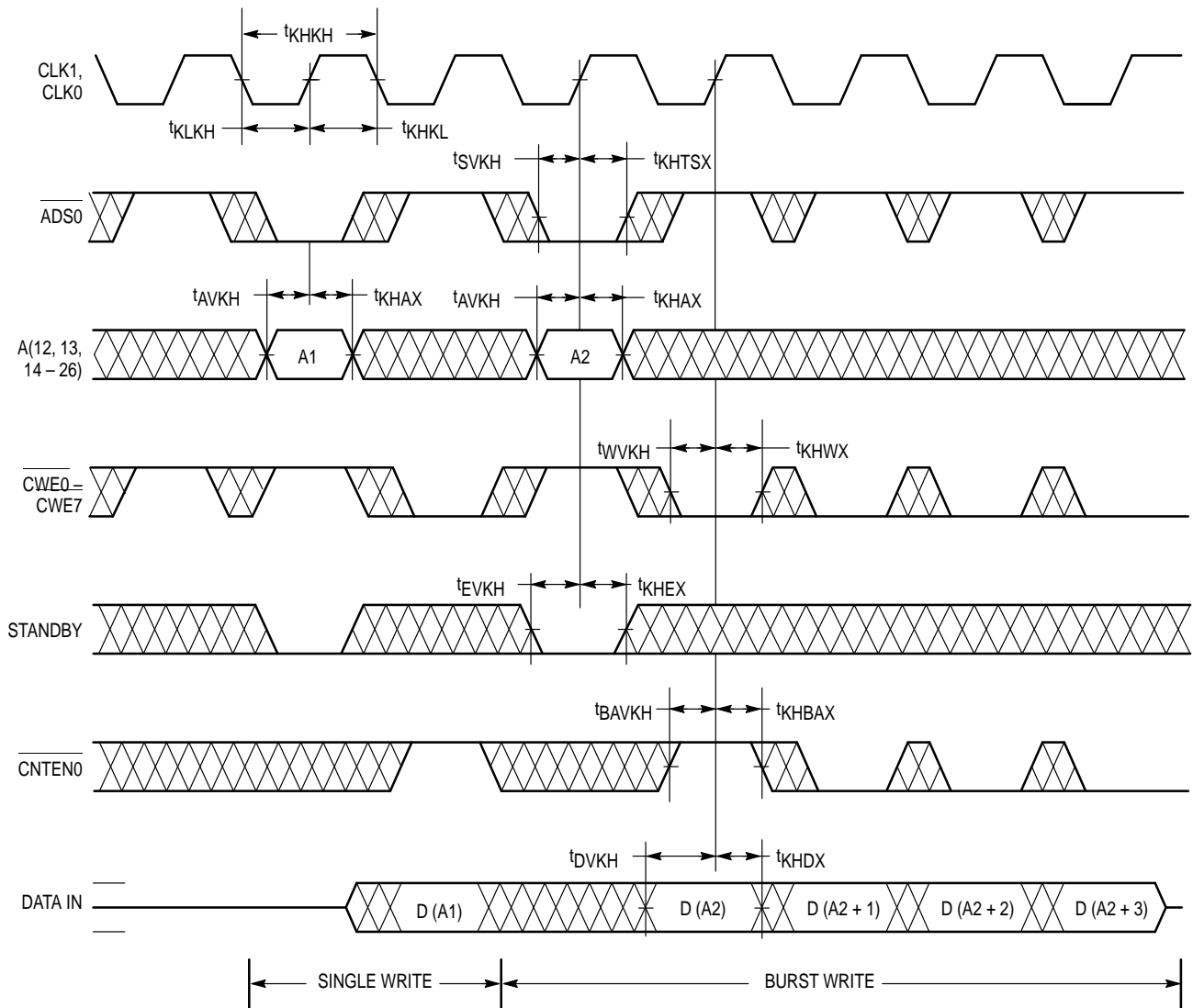
SYNCHRONOUS DATA RAM READ CYCLE



NOTES:

1. Cache addresses used are: 14 – 26 for MPC2104 and MPC2107; 13 – 26 for MPC2105; and 12 – 26 for MPC2106.
2. Q1 (A2) represents the first output from the external address A2; Q2 (A2) represents the next output data in the burst sequence with A2 as the base address.

SYNCHRONOUS DATA RAM WRITE CYCLE



NOTES:

1. Cache addresses used are: 14 – 26 for MPC2104 and MPC2107; 13 – 26 for MPC2105; and 12 – 26 for MPC2106.
2. $COE0 = V_{IH}$

AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = 5.0\text{ V} \pm 5\%$ $T_A = 0\text{ to } +70^\circ\text{C}$, Unless Otherwise Noted)

Input Timing Measurement Reference Level 1.5 V Output Timing Reference Level 1.5 V
 Input Pulse Levels 0 to 3.0 V Output Load See Figure 1A Unless Otherwise Noted
 Input Rise/Fall Time 3 ns

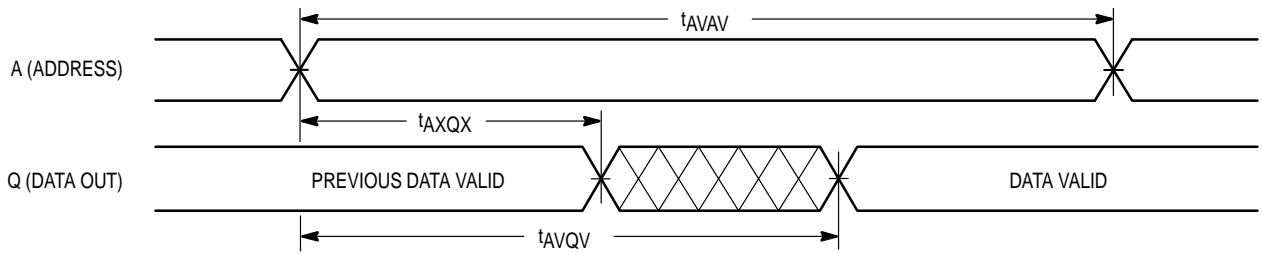
ASYNCHRONOUS DATA RAMs READ CYCLE TIMING (See Notes 1 and 8)

| Parameter | Symbol | MPC2107-15 | | Unit | Notes |
|-------------------------------------|--------------|------------|-----|------|---------|
| | | Min | Max | | |
| Cycle Time | t_{AVAV} | 15 | — | ns | 2 |
| Address Access Time | t_{AVQV} | — | 15 | ns | |
| Enable Access Time | t_{ELQV} | — | 15 | ns | 3 |
| Output Enable Access Time | t_{GLQV} | — | 8 | ns | |
| Output Hold from Address Change | t_{AXQX} | 4 | — | ns | 4, 5, 6 |
| Enable Low to Output Active | t_{ELQX} | 4 | — | ns | 4, 5, 6 |
| Enable High to Output High-Z | t_{EHQZ} | 0 | 8 | ns | 4, 5, 6 |
| Output Enable Low to Output Active | t_{GLQX} | 0 | — | ns | 4, 5, 6 |
| Output Enable High to Output High-Z | t_{GHQZ} | 0 | 7 | ns | 4, 5, 6 |
| Power Up Time | t_{ELICCH} | 0 | — | ns | |
| Power Down Time | t_{EHICCL} | — | 15 | ns | |

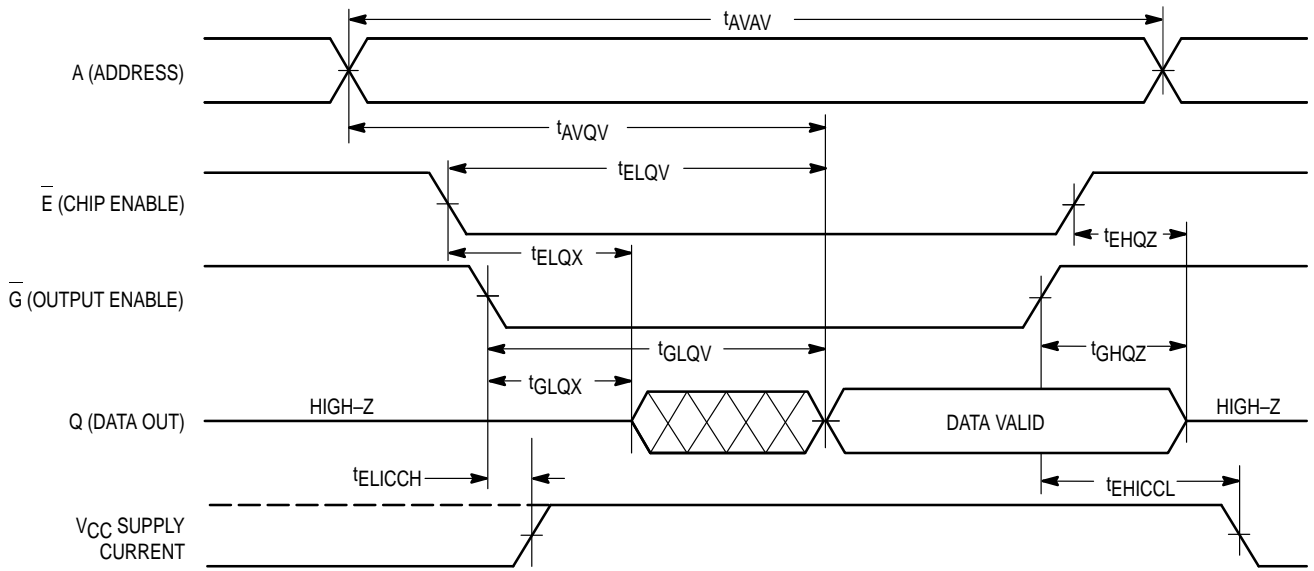
NOTES:

1. W is high for read cycle.
2. All timings are referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with E going low.
4. At any given voltage and temperature, $t_{EHQZ}(\text{max})$ is less than $t_{ELQX}(\text{min})$, and $t_{GHQZ}(\text{max})$ is less than $t_{GLQX}(\text{min})$, both for a given device and from device to device.
5. Transition is measured $\pm 500\text{ mV}$ from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($E = V_{IL}$, $COE0 = V_{IL}$).
8. Applies to MPC2107.

ASYNCHRONOUS READ CYCLE 1 (See Note 7)



ASYNCHRONOUS READ CYCLE 2 (See Note 3)



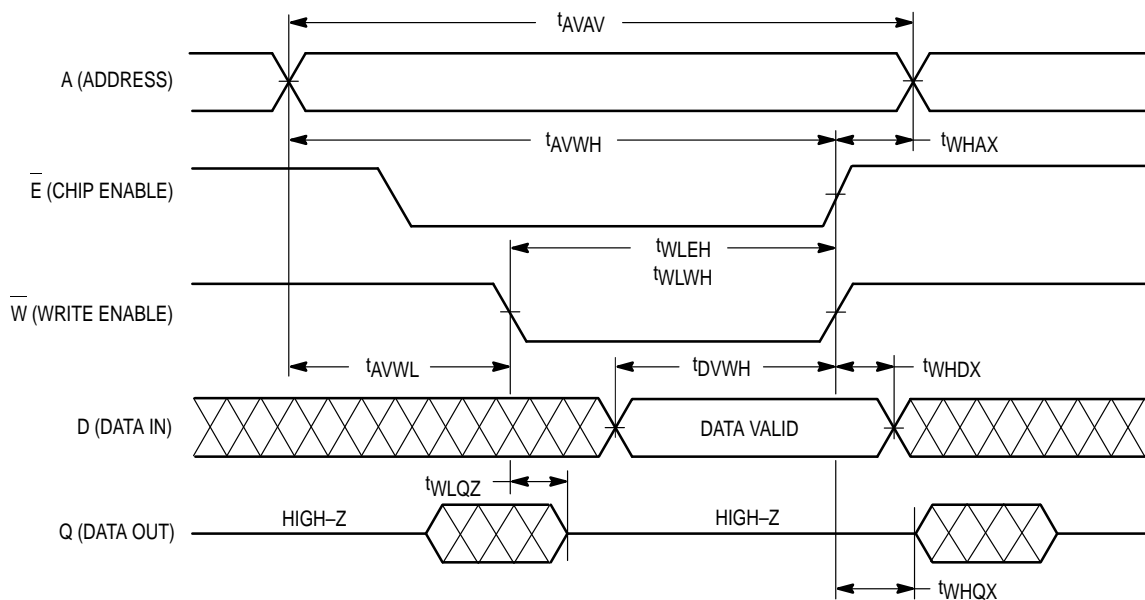
ASYNCHRONOUS DATA RAMs WRITE CYCLE 1 (See Notes 1 and 2)

| Parameter | Symbol | MPC2107-15 | | Unit | Notes |
|-------------------------------|--------------------------|------------|-----|------|-------|
| | | Min | Max | | |
| Write Cycle Time | t_{AVAV} | 15 | — | ns | 3 |
| Address Set-up Time | t_{AVWL} | 0 | — | ns | |
| Address Valid to End of Write | t_{AVWH} | 12 | — | ns | |
| Write Pulse Width | t_{WLWH} t_{WLEH} | 12 | — | ns | |
| Write Pulse Width, G High | t_{WLWH} t_{WLEH} | 10 | — | ns | 4 |
| Data Valid to End of Write | t_{DVWH} | 7 | — | ns | |
| Data Hold Time | t_{WHDX} | 0 | — | ns | |
| Write Low to Output High-Z | t_{WLQZ} | 0 | 7 | ns | 5,6,7 |
| Write High to Output Active | t_{WHQX} | 5 | — | ns | 5,6,7 |
| Write Recovery Time | t_{WHAX} | 0 | — | ns | |

NOTES:

1. A write occurs during the overlap of \bar{E}_{low} and \bar{W}_{low} .
2. If \bar{E} goes low coincident with or after \bar{W} goes low, the output will remain in a high impedance state.
3. All timings are referenced from the last valid address to the first transitioning address.
4. If $\bar{E} \geq V_{IH}$, the output will remain in a high impedance state.
5. At any given voltage and temperature, t_{WLQZ} (max) is less than t_{WHQX} (min), both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.

ASYNCHRONOUS WRITE CYCLE 1 (\bar{W} Controlled, See Notes 1 and 2)



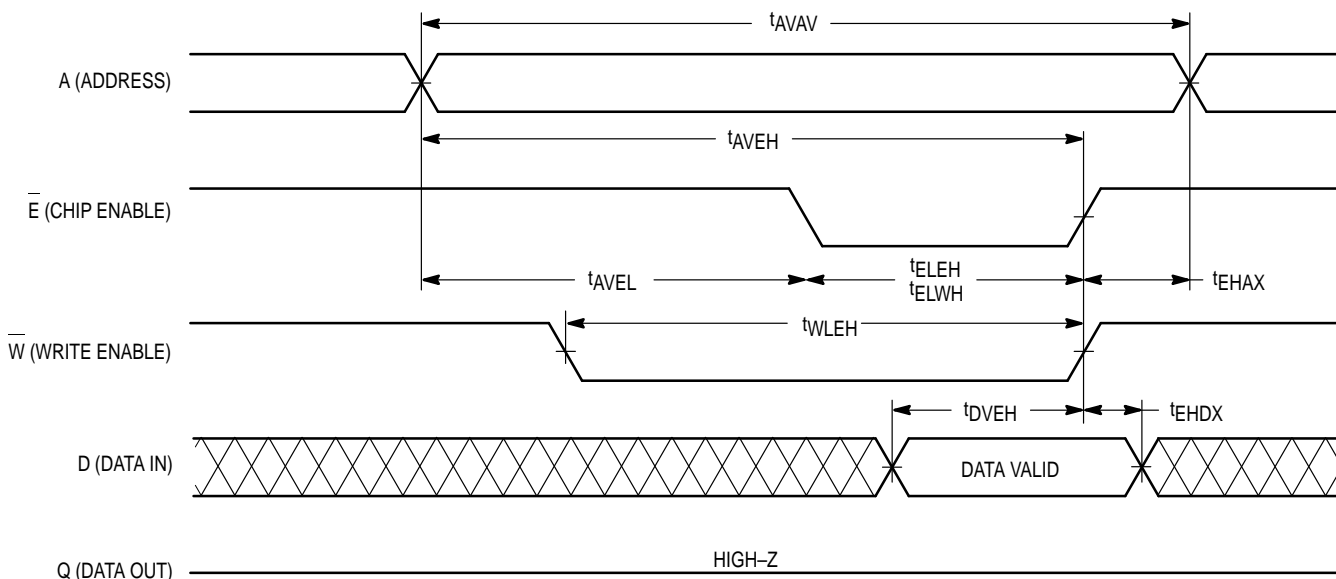
ASYNCHRONOUS DATA RAMs WRITE CYCLE 2 (\bar{E} Controlled, See Notes 1 and 2)

| Parameter | Symbol | MPC2107-15 | | Unit | Notes |
|-------------------------------|--------------------------|------------|-----|------|-------|
| | | Min | Max | | |
| Write Cycle Time | t_{AVAV} | 15 | — | ns | 0 |
| Address Setup Time | t_{AVEL} | 0 | — | ns | |
| Address Valid to End of Write | t_{AVEH} | 12 | — | ns | |
| Enable to End of Write | t_{ELEH} t_{ELWH} | 10 | — | ns | 3, 4 |
| Data Valid to End of Write | t_{DVEH} | 7 | — | ns | |
| Data Hold Time | t_{EHDX} | 0 | — | ns | |
| Write Recovery Time | t_{EHAX} | 0 | — | ns | |

NOTES:

1. A write occurs during the overlap of \bar{E} low and \bar{W} low.
2. All timings are referenced from the last valid address to the first transitioning address.
3. If \bar{E} goes low coincident with or after \bar{W} goes low, the output will remain in a high impedance state.
4. If \bar{E} goes high coincident with or before \bar{W} goes high, the output will remain in a high impedance state.

ASYNCHRONOUS WRITE CYCLE 2 (\bar{E} Controlled, See Note 1)



TAG RAM

RESET FUNCTION TRUTH TABLE (See Notes 1 and 2)

| TCLR | CLK | TWE | TAG | VLD _{out} | DTY _{out} | WT _{out} | MATCH | TA | Operation | POWER |
|------|-----|-----|--------|--------------------|--------------------|-------------------|------------------|--------|--------------|--------|
| L | L-H | H | High-Z | L ⁽³⁾ | L ⁽³⁾ | L ⁽³⁾ | L ⁽³⁾ | High-Z | Reset Status | Active |
| L | L-H | L | — | — | — | — | — | — | Not Allowed | — |

NOTES:

- H = V_{IH}, L = V_{IL}, X = don't care, — = unrelated.
- TOE is X for this table.

READ FUNCTION TRUTH TABLE (See Notes 1, 2, and 3)

| TOE | TWE | CLK | TAG | VLD _{in} | DTY _{in} | WT _{in} | VLD _{out} | DTY _{out} | WT _{out} | MATCH | Operation |
|-----|-----|-----|------------------|-------------------|-------------------|------------------|--------------------|--------------------|-------------------|------------------|-----------------|
| L | H | X | D _{OUT} | — | — | — | — | — | — | D _{OUT} | Read Tag I/O |
| H | X | X | High-Z | — | — | — | — | — | — | — | Tag I/O Disable |

WRITE FUNCTION TRUTH TABLE (See Notes 1 and 2)

| TOE | TWE | CLK | TAG | VLD _{in} | DTY _{in} | WT _{in} | VLD _{out} | DTY _{out} | WT _{out} | MATCH | Operation |
|-----|-----|-----|-----------------|-------------------|-------------------|------------------|--------------------|--------------------|-------------------|-------|---------------|
| H | L | L-H | D _{IN} | — | — | — | D _{OUT} | D _{OUT} | D _{OUT} | L | Write Tag I/O |
| L | L | L-H | — | — | — | — | — | — | — | — | Not Allowed |

NOTES:

- H = V_{IH}, L = V_{IL}, X = don't care, — = unrelated.
- This table applies when RESET and PWRDN are high.
- D_{OUT} in this case is the same as D_{IN}. The input data is written through to the outputs during the write operation.

MATCH FUNCTION TRUTH TABLE (See Notes 1 through 4)

| TOE | TWE | TAG | VLD ⁽⁴⁾ | DTY ⁽⁴⁾ | WT ⁽⁴⁾ | MATCH | Operation |
|-----|-----|-------------------|--------------------|--------------------|-------------------|------------------|--------------------------------------|
| X | X | — | — | — | — | D _{OUT} | Selected |
| L | H | D _{OUT} | — | — | — | L | Read Tag I/O |
| H | L | D _{IN} | D _{IN} | D _{IN} | D _{IN} | L | Write Tag I/O, Status Bits |
| H | H | TAG _{IN} | L | — | — | L | Invalid Data – Dedicated Status Bits |
| H | H | TAG _{IN} | H | — | — | M | Match – Dedicated Status Bits |

NOTES:

- H = V_{IH}, L = V_{IL}, X = don't care, — = unrelated.
- M = high if TAG_{IN} equals the memory contents at the address; M = low if TAG_{IN} does not equal the contents at that address.
- PWRDN and RESET are high for this table. OES and CLK are X.
- This column represents the stored memory cell data for the given status bit at the selected address.

TAG RAM AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = 5.0\text{ V} \pm 5\%$, $T_A = 0\text{ to } +70^\circ\text{C}$, Unless Otherwise Noted)

Input Timing Measurement Reference Level 1.5 V
 Input Pulse Levels 0 to 3.0 V
 Input Rise/Fall Time 3 ns

Output Timing Measurement Reference Level 1.5 V
 Output Load Figure 1A Unless Otherwise Noted

TAG RAM READ CYCLE (See Notes 1 through 4)

| Parameter | Symbol | Tag RAM | | Unit | Notes |
|-------------------------------------|------------|---------|-----|------|-------|
| | | Min | Max | | |
| Clock Access Time | t_{KHQV} | — | 10 | ns | |
| Output Enable to Output Valid | t_{GLQV} | — | 8 | ns | |
| Output Enable to Output Active | t_{GLQX} | 0 | — | ns | |
| Output Disable to Q High-Z | t_{GHQZ} | 1 | 6 | ns | |
| Status Bit Hold from Address Change | t_{AXSX} | 3 | — | ns | |
| Address Access Time Status Bits | t_{AVSV} | — | 10 | ns | |
| Tag Bit Hold from Address Change | t_{AVQX} | 3 | — | ns | |
| Address Access Time Tag Bits | t_{AVQV} | — | 12 | ns | |

NOTES:

1. Set-up and hold times, W (write) refers to TWE.
2. A read cycle is defined by TWE high. A write cycle is defined by TWE low.
3. Maximum access times are guaranteed for all possible MC68040 and PowerPC external bus cycles.
4. Tag reads are asynchronous.

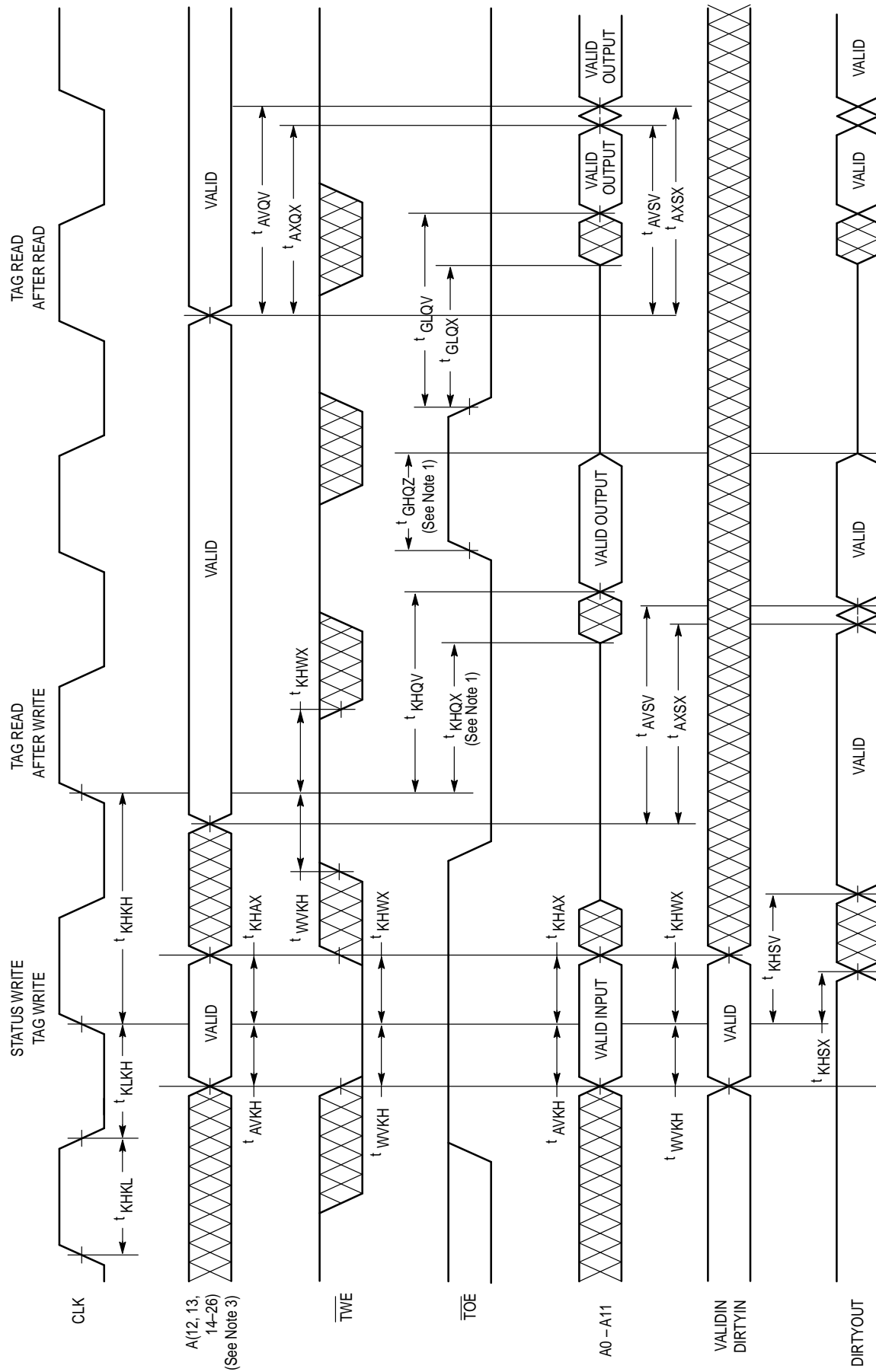
TAG RAM WRITE CYCLE (See Notes 1 through 4)

| Parameter | Symbol | Tag RAM | | Unit | Notes |
|---------------------------------|---|---------|-----|------|-------|
| | | Min | Max | | |
| Cycle Time | t_{KHKH} | 15 | — | ns | |
| Clock High Pulse Width | t_{KHKL} | 4.5 | — | ns | |
| Clock Low Pulse Width | t_{KLKH} | 4.5 | — | ns | |
| Clock High to Output Active | t_{KHQX} | 1.5 | — | ns | |
| Set-up Times | Address Write t_{AVKH} t_{WVKH} | 3 | — | ns | |
| Hold Times | Address Write t_{KHAX} $t_{KH WX}$ | 1.5 | — | ns | |
| Status Output Hold | t_{KHSX} | 0 | — | ns | |
| Clock High to Status Bits Valid | t_{KHSV} | — | 9 | ns | |

NOTES:

1. Set-up and hold times, W (write) refers to TWE.
2. A read cycle is defined by TWE high. A write cycle is defined by TWE low.
3. Maximum access times are guaranteed for all possible MC68040 and PowerPC external bus cycles.
4. Tag writes are synchronous.

TAG RAM WRITE AND READ CYCLES (See Note 2)



NOTE:

1. Transition is measured plus or minus 200 mV from steady state.
2. $TCLR = High$.
3. Cache addresses used are: 14-26 for MPC2004 and MPC2007; 13-26 for MPC2005; 12-26 for MPC2006 and MPC2009.

TAG RAM MATCH CYCLE

| Parameter | Symbol | Tag RAM | | Unit | Notes |
|--------------------------------------|-------------------|---------|-----|------|-------|
| | | Min | Max | | |
| Clock High Write to MATCH Invalid | t _{KHML} | — | 7 | ns | |
| Clock High Read to MATCH Valid | t _{KHMV} | — | 10 | ns | |
| Address Valid to MATCH Valid | t _{AVMV} | — | 10 | ns | |
| MATCH Valid Hold from Address Change | t _{AXMX} | 2 | — | ns | |
| TOE Low to MATCH Invalid | t _{GLML} | — | 7 | ns | |
| TOE High to MATCH Valid | t _{GHMX} | — | 8 | ns | |

TAG RAM RESET (TCLR) CYCLE

| Parameter | Symbol | Tag RAM | | Unit | Notes |
|-------------------------------|-------------------|---------|-----|------|-------|
| | | Min | Max | | |
| TCLR Set-up Time | t _{STC} | 4 | — | ns | |
| TCLR Hold Time | t _{HTC} | 1 | — | ns | |
| Status Bit Reset Time | t _{SRST} | — | 60 | ns | |
| Status Bit Hold from TCLR Low | t _{SHRS} | 2 | — | ns | |
| TCLR Low to MATCH Invalid | t _{RSML} | — | 10 | ns | |
| TCLR High to MATCH Valid | t _{RSMV} | — | 100 | ns | |
| TCLR Low to TAG High-Z | t _{RSQZ} | — | 10 | ns | |
| TCLR High to TAG Active | t _{RSQX} | — | 100 | ns | |
| STANDBY Set-up to TCLR Low | t _{PDSR} | 30 | — | ns | |
| TCLR High to TWE Low | t _{RHWX} | 80 | — | ns | |

AC TEST LOADS

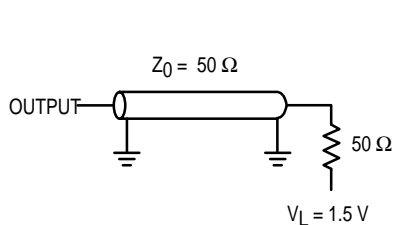


Figure 1A

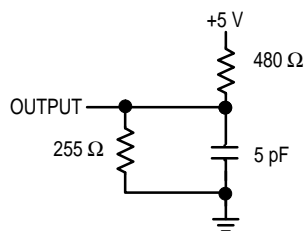
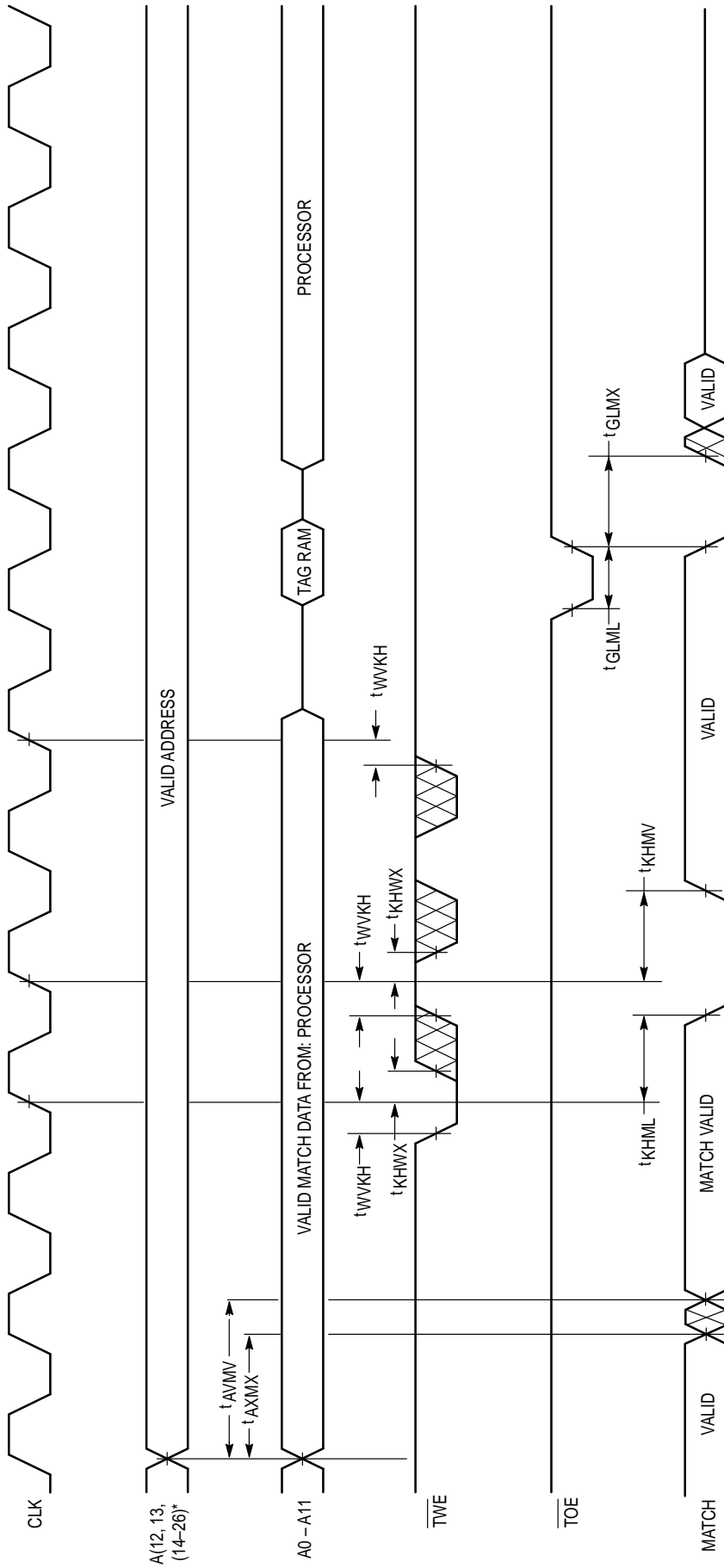


Figure 1B

TIMING LIMITS

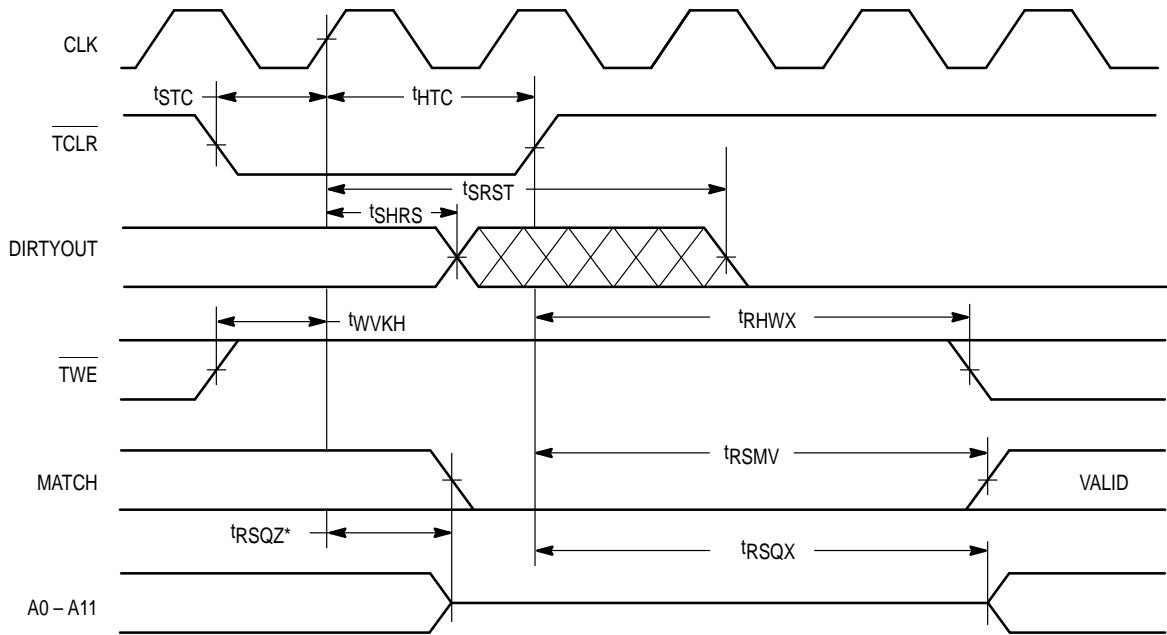
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

TAG RAM MATCH CYCLE



* Cache addresses used are: 14-26 for MPC2004 and MPC2007; 13-26 for MPC2005; 12-26 for MPC2006.

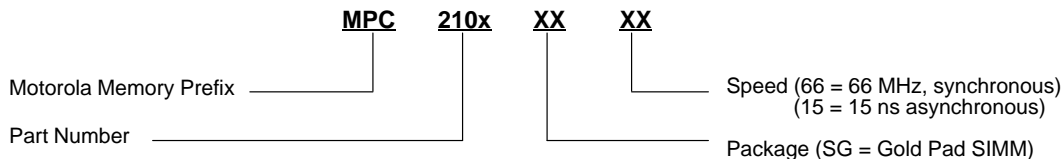
TAG RAM TCLR FUNCTION



* Transition is measured plus or minus 200 mV from steady state.


ORDERING INFORMATION

(Order by Full Part Number)



Full Part Numbers — MPC2104SG66
MPC2105SG66
MPC2106SG66
MPC2107SG15

MPC2104 = 256KB, synchronous
MPC2105 = 512KB, synchronous
MPC2106 = 1MB, synchronous
MPC2107 = 256KB, asynchronous

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